Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V+**
2. **OFFSET ADJ**
3. **INPUT**
4. **V-**
5. **OUTPUT**
6. **CH**
7. **LOGIC REF**
8. **LOGIC**

**.062”**

**.077”**

**FUSE LINK**

**SENSE**

**6**

**7**

**8**

**1**

**2**

**3 4**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .062” X .077” DATE: 1/10/19**

**MFG: LINEAR TECH THICKNESS .012” P/N: LF398**

**DG 10.1.2**

#### Rev B, 7/1